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2006-1230 (SERIAL NO. 09/885,217)

Johnson/Picco/6

In The United States Court of Appeals For The Federal Circuit

IN RE MICRON TECHNOLOGY, INC.

APPEAL FROM THE UNITED STATES PATENT AND TRADEMARK OFFICE, BOARD OF PATENT APPEALS AND INTERFERENCES.

BRIEF OF APPELLANT

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Dated: April 7, 2006

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FORM 9. Certificate of Interest

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

In re: Micron Technology, Inc. v. _____

No. 2006-1230

CERTIFICATE OF INTEREST

Counsel for the (petitioner) (appellant) (respondent) (appellee) (amicus) (name of party) Micron Technology, Inc. certifies the following (use "None" if applicable; use extra sheets if necessary):

1. The full name of every party or amicus represented by me is:

Micron Technology, Inc.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

Brandes Investment Partners, LP

Capital Research and Management Co.

4. ☐ There is no such corporation as listed in paragraph 3.

5. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

Thorp Reed & Armstrong -- Edward L. Pencoske

Jones Day -- Edward L. Pencoske

February 22, 2006
Date

Signature of counsel

Edward L. Pencoske
Printed name of counsel

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STATEMENT OF RELATED CASES

No appeal in or from this matter was previously before this or any other appellate court.

Counsel is not aware of any case pending in this or any other court that will directly affect or be directly affected by this court's decision in the pending appeal.

JURISDICTIONAL STATEMENT

This is an appeal from a final decision of the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office dated 31 October 2005 with respect to a patent application. An appeal from the Board's adverse decision was timely filed with this court on 29 December 2005. This court has jurisdiction pursuant to 28 U.S.C. § 1295(a)(4)(A).

STATEMENT OF THE ISSUES

I. WHETHER THE BOARD'S CONCLUSION THAT THE PRIOR ART (U.S. PATENT NO. 5,757,175 TO MORISHITA ET AL. ("MORISHITA")) DISCLOSES A UNITY GAIN AMPLIFIER IS SUPPORTED BY SUBSTANTIAL EVIDENCE.

II. WHETHER THE BOARD'S CLAIM CONSTRUCTION IN WHICH TWO LIMITATIONS OF THE CLAIM WERE SATISFIED BY THE SAME TEACHING IN THE PRIOR ART WAS UNREASONABLE.

STATEMENT OF THE CASE

This case is on appeal from a decision of the Patent and Trademark Office's Board of Patent Appeals and Interferences affirming the final rejection of claims 223, 225, 228 - 237, 247 - 250, 496, and 499 - 515 on the basis of prior art. The primary reference relied upon by the examiner in rejecting the claims was U.S. Patent No. 5,757,175 to Morishita et al. ("Morishita"). More particularly, the examiner found that Morishita discloses a unity gain amplifier. The Board agreed with the examiner that Morishita discloses a unity gain amplifier and affirmed the rejection of claims 223, 225, 228 – 237, 247 – 250, 496, and 499 – 515. Appellants' contend that Morishita does not disclose a unity gain amplifier. Appellants' also contend that the Board's construction of two different limitations in claim 223 to mean the same thing was unreasonable.

STATEMENT OF THE FACTS

The patent application discloses an apparatus and method for generating a reference voltage for use in a memory circuit. An exemplary embodiment of the invention is found at JP00085. A description of the operation of that circuit is found at JP00086-JP00094, although a detailed understanding of the operation of the circuit is not necessary to decide the issues presented by this appeal. Suffice it to say that the invention is a circuit that produces a very stable reference voltage in response to the application of an externally supplied voltage or signal.[1]

For purposes of this appeal, claim 223 may be treated as the representative claim. Claim 223 recites:

> A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:
>
> an active reference circuit for receiving the external voltage and for producing a reference signal *having a desired relationship with the external signal*, said active reference circuit comprising a current source utilizing a current mirror for providing current to a diode stack having an adjustable impedance, *wherein said reference signal is dependent upon said external voltage*; and
>
> *a unity gain amplifier* responsive to said reference signal for producing the reference voltage. (Emphasis added.) (JP00076)

[1] The reader desiring a description of the operation of the circuit shown in JP00085 is directed to the Summary of the Invention, found in Appellant's Brief Before the Board of Patent Appeals and Interferences. JP00071-JP00072.

Note that claim 223 recites a unity gain amplifier. A unity gain amplifier is an amplifier having a gain of "unity" such that the output signal is the same magnitude as the input signal. The advantage of passing a signal through a unity gain amplifier is to improve the voltage characteristics of the signal. JP00091. Note also that the reference signal has *a desired relationship with the external signal* and *is dependant upon the external voltage* [signal].

After a long prosecution history, which is not relevant to any issue on appeal, certain claims were finally rejected in an Office action dated November 13, 2003. JP00101 - JP00113. Specifically: Claims 223 and 511 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by Morishita. Claims 225, 496, 499, 500, and 514 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Morishita in view of Zarrabian (U.S. Patent no. 5,838,076). Claims 228-230 and 501-503 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Morishita in view of Park (U.S. Patent no. 5,448,199). Claims 231, 504, 512, and 515 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsay (U.S. Patent No. 6,127,881) in view of Morishita. Claims 232, 233, 505, and 506 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayakawa (U.S. Patent No. 5,184,031) in view of Tsay and Morishita. Claims 234-237, 247-250, 507-510, and 513 were finally rejected

under 35 U.S.C. § 103(a) as being unpatentable over Hayakawa in view of Tsay, Morishita, and Park. JP00002-JP00003.

Morishita was the primary reference relied upon by the examiner. The crux of the examiner's position was that elements CMP and DT of Morishita's figure 17 (JP00234) disclose a unity gain amplifier. Applicants timely filed an appeal to the Board of Patent Appeals and Interferences ("Board").

Before the Board, claim 223 was selected as the representative claim for all claims on appeal. JP00004. Applicants' primary argument was that Morishita did not disclose a unity gain amplifier. JP00072. The Board, however, affirmed the rejection of the claims stating that they found no error in the Examiner's position that the elements CMP and DT in Morishita form a unity gain amplifier. JP00026 - JP00027. Applicants' other argument, that the reference signal have *a desired relationship with the external signal* and that the reference signal be *dependent upon said external voltage* [signal] was disposed by the Board as follows: "the fact alone that a reference voltage in Morishita may not be produced until an external voltage exceeds a prescribed level establishes, in our view a desired relationship with such external voltage. Similarly, the reliance on the attaining of a voltage level by the external voltage in Morishita before a reference voltage is produced makes Morishita's reference voltage dependent on the external voltage as claimed." JP00027 - JP00028.

Morishita is the primary reference relied upon by the Office in rejecting all of the claims. JP00002 – JP00003. If this court should determine that the Board's conclusion that Morishita discloses a unity gain amplifier is not supported by substantial evidence (and it is not), or that the phrases "desired relationship" and "dependant upon" do not mean the same thing (and they don't), then the decision of the Board must be reversed.

SUMMARY OF THE ARGUMENT

I. The Board is just plain wrong. The portions of Morishita relied upon for a teaching of a unity gain amplifier disclose a comparator (CMP) and a drive or switching transistor (DT) responsive to the comparator. Morishita, on its face, calls the amplifier a comparator, and the Office has introduced no evidence that combining a comparator with a drive transistor forms a unity gain amplifier. Morishita doesn't call the combination of the comparator and the drive transistor a unity gain amplifier, and the combination of the comparator and the drive transistor does not form a unity gain amplifier. Because Morishita does not disclose a unity gain amplifier, the Board has not made out a prima facie case of anticipation; the Board must be reversed.

II. The Board erred by using a single teaching to satisfy two separate limitations in the claim. In effect, the Board construed the two limitations to be the same and thus taught by a single teaching in the art. The Board's claim construction is unreasonable and must be reversed.

ARGUMENT

I. MORISHITA DOES NOT DISCLOSE A UNITY GAIN AMPLIFIER.

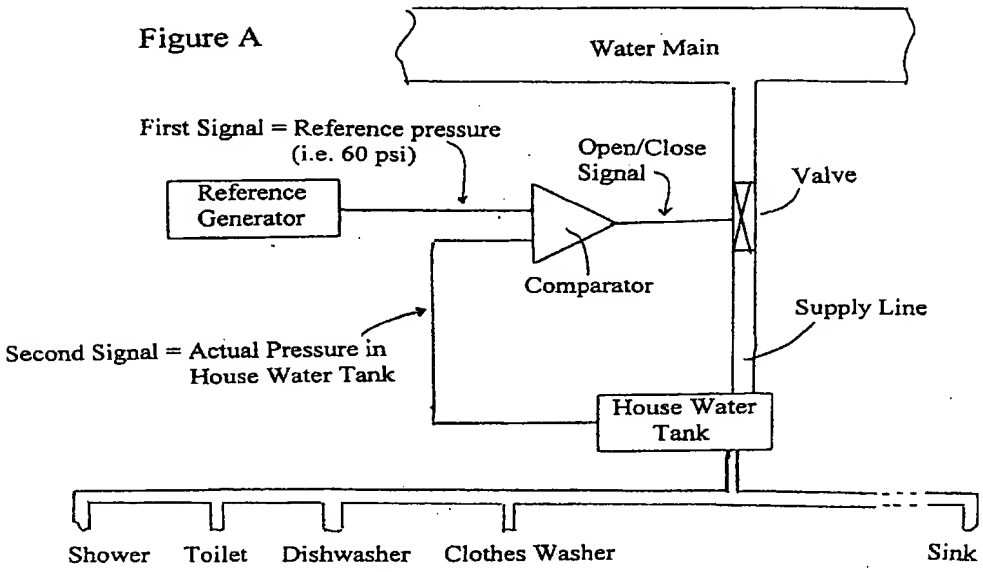
A. The standard of review

Appellant is challenging a factual finding of the Board, i.e., that Morishita discloses a unity gain amplifier. Factual findings by the Board should be affirmed only if they are supported by substantial evidence. In re Hyatt, 211 F.3d 1367, 54 USPQ 2d 1664 (Fed. Cir. 2000); In re Gartside, 203 F.3d 1305, 53 USPQ 2d 1769 (Fed. Cir. 2000)

B. A simple analogy

The Board relies upon figures 17-19 of Morishita. However, before discussing figure 17 of Morishita, a simple analogy represented in Figure A below is discussed.

Figure A



In Figure A, a house water tank is illustrated. The house water tank provides water to a shower, a toilet, a dishwasher, a sink, and other appliances requiring water. Of course, the demands for water from the water tank are variable depending upon which appliances may be turned on at any given time. The house water tank is connected to a water main through a supply pipe having a valve positioned therein. The water main may be viewed as a limitless supply of water having a very high water pressure. However, water in the house water tank is maintained, for example, at 60 psi (pounds per square inch) so that the various appliances may operate properly.

Figure A also includes a comparator. The comparator receives two signals. A first signal is representative of a desired, reference pressure, i.e., 60 psi, that should be in the house water tank. The first signal does not change. The second signal is representative of the actual pressure in the house water tank. That signal will change depending on the demand for water. The comparator compares these two signals, and produces an open/close signal which is used to control the valve in the supply line.

In operation, let us assume that the house water tank is full, and the pressure in the tank is 60 psi. Under those conditions, when the comparator compares the first signal to the second signal, i.e., desired pressure in the house water tank (60 psi) with the actual pressure in the water tank (60 psi), the comparator determines

that no additional water needs to be added to the house water tank. Under those conditions, the open/close signal has a value of zero, and the valve is closed.

Now, let us assume that someone begins to take a shower. As the shower is operated, the house water tank begins to drain and the pressure falls below 60 psi. The comparator, upon seeing that the actual pressure in the house water tank is now below the desired pressure of 60 psi, produces an open/close signal having a small value, so that the valve in the supply line will be opened a small amount. With the valve now opened a small amount, water from the water main begins flowing into the house water tank to replace the water that is flowing out for the shower.

Assume now that the toilet is flushed, and as a result of the large demand for water, there is a large drop in the pressure in the house water tank. The comparator now sees that the actual pressure in the house water tank is much lower than the desired pressure of 60 psi and produces an open/close signal having a larger magnitude so that the valve in the supply line is opened even more, so that more water from the water main may flow into the house water tank. After the toilet is refilled, and the shower has ended, the pressure in the house water tank will eventually return to 60 psi. At that point, the comparator determines that the actual pressure in the house water tank (60 psi) is equal to the desired reference pressure

(60 psi) and produces a signal to close the valve in the supply line. Figure 17 of Morishita operates the same way.

In figure 17, an amplifier is set up to operate as a comparator (CMP). JP00234, JP00236 The amplifier CMP receives a reference voltage which is representative of the desired voltage on the power supply line (PSL) (which is analogous to the house water tank). As the internal circuit (INC) draws current from the power supply line (PSL), the voltage on that line begins to drop. The comparator (CMP), seeing the drop in voltage on the power supply line as compared to the desired reference voltage, issues a signal to the transistor DT (analogous to the valve in the water supply line) to begin conducting current from the external voltage supply so as to increase the voltage on the power supply line (PSL). When the voltage on the power supply line (PSL) is equal to the reference voltage, the output of the amplifier CMP is zero, and the transistor DT is turned off. That is what is taught by Morishita, beginning at column 1, line 66 and continuing to column 2, line 37, which provides:

> FIG. 17 schematically shows the structure of a conventional internal power supply down-converter. In FIG. 17, the internal power supply down-converter includes a reference voltage generating circuit VRG operating with an external power supply voltage EXVcc and a ground voltage Vss as both operating power supply voltages for generating a reference voltage Vref, a comparator CMP operating with the external power supply voltage EXVcc and the ground voltage Vss as both operating power supply voltages for comparing the

> reference voltage Vref with an internal power supply voltage INVcc on an internal power supply line PSL, a driver transistor DT constituted by a p channel MOS transistor responsive to an output signal of comparator CMP for supplying current from an external power supply node EXVcc (a power supply node and a voltage applied thereto are herein denoted with the same reference character) to internal power supply line PSL. JP00236.

C. The Examiner's reasoning is flawed

It is the Examiner's position that figure 17 of Morishita "shows a unity gain amplifier (CMP, DT) responsive to the reference signal for producing the reference voltage." JP00057. Although Morishita never calls the combination of the comparator CMP and driver (DT) a unity gain amplifier, the examiner concluded:

> The gain of amplifier circuit, which comprises elements CMP and DT, is the ratio of INVCC voltage and Vref voltage (gain = Vout/Vin). As cited by Applicant, Morishita et al. states in column 2, lines 21-34, that ". . . This internal power supply down-converter therefore maintains the internal power supply voltage INVcc at the reference voltage Vref level." Thus, INVcc is equal to Vref. Therefore, the gain of the amplifier, which comprises elements CMP and DT, is one (1) or unity. (emphasis in original) JP00063 - JP00064.

The Examiner's logic is simply incorrect. Simply because, at some point in time, two signals may be equal to one another does not mean that all of the circuitry between those two signals is a unity gain amplifier.

Return again to our analogy of the water system in Fig. A. Assume that a substantial number of the appliances have been turned on such that the pressure in

the house water tank falls to 30 psi. Under those conditions, the comparator will see a huge difference between the desired water pressure of 60 psi and the actual water pressure of 30 psi such that it will produce a large signal so that the valve in the supply line is opened, perhaps to its full extent. Under those conditions, the gain will be substantially large and, depending upon the pressure on the water main, much more than unity. As the pressure in the house water tank begins to approach 60 psi, the signal produced by the comparator will begin to decrease in value, thereby slowly closing the valve such that the gain will be gradually reduced from its maximum value. At some point, when the desired pressure of 60 psi and the actual pressure in the water tank are equal, the signal produced by the comparator will be reduced to zero and the valve in the supply line will be closed. At that time, the gain is zero. Thus, it cannot be said that the combination of the comparator and the valve are a unity gain amplifier simply because at some point in time the actual pressure in the house water tank is equal to the desired reference pressure.

The same is true of the circuit of Morishita. The combination of the comparator and the transistor DT cannot be viewed as a unity gain amplifier because, should the voltage on the power supply line (PSL) be substantially lower than the reference voltage, the signal produced by the comparator will be very large, and the transistor DT will be fully conductive. Under those conditions, the

gain of the comparator and the transistor will be greater than one. At the other extreme, when the voltage on the power supply line (PSL) is equal to the reference voltage, the signal produced by the comparator is zero, the transistor DT is non-conductive, and the gain of the two components is zero. Thus, the combination of the comparator and the transistor DT is simply not a unity gain amplifier.

D. The Board's conclusion that Morishita discloses a unity gain amplifier is not supported by any evidence.

Perhaps the Board was concerned about the accuracy of the Examiner's reasoning when they stated "we are in *general* agreement with the Examiner's position as stated in the Answer." (Emphasis added) JP00006. The Board went on to state:

> We find no arguments from Appellants that convince us of any error in the Examiner's position which, considering the entire circuitry illustrated in Figure 17 in Morishita as a voltage reference circuit, asserts that the amplifier circuit comprising elements CMP and DT in Morishita is a unity gain amplifier. We further agree with the Examiner that Morishita's unity gain amplifier produces a reference voltage as claimed since the reference voltage Vref is maintained at the internal power supply voltage INVcc level.

While we are aware that this court reviews decisions and not opinions, the foregoing statement illustrates the Board's failure to understand the operation of Morishita and, thus, why it came to affirm the Examiner. In fact, the circuit of Morishita operates in exactly the *opposite* manner as stated by the Board. More

specifically, the internal power supply voltage INVcc is maintained at the level of Vref, and not the other way around. The Board's failure to understand which voltage is being controlled or regulated, and which of the voltages is fixed, clearly underlies the Board's failure to comprehend how the circuit shown in figure 17 of Morishita is operating. Furthermore, Morishita calls component CMP a comparator. It produces a signal representative of the difference between the two signals input thereto. JP00236 (column 2, lines 21-25). Combining the output of a comparator with a drive transistor, which is nothing more than a switch, cannot possibly create a unity gain amplifier. The Office has introduced no evidence to support its position that a drive transistor responsive to a comparator forms a unity gain amplifier. There is nothing in this combination of components which takes a single input signal and multiplies that single input signal by unity.

The parties agree that anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention, as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). JP00005.

In this case, Appellants have demonstrated based on the express teaching of Morishita itself that the comparator CMP and transistor DT operate to provide variable gain, anywhere from zero up through some unspecified number (beyond unity), depending upon how much voltage is being drawn from the power supply line (analogous to how much water is being drawn from the house water tank). There is no evidence to support the Board's conclusion that the comparator CMP and transistor DT in Morishita are a unity gain amplifier. Therefore, the Board has failed to make out a prima facie case of anticipation; the rejection of claim 223 as being anticipated by Morishita must be reversed.

II. THAT THE CIRCUIT OF MORISHITA DOES NOT BEGIN TO OPERATE UNTIL A CERTAIN VOLTAGE IS REACHED, DOES NOT TEACH THAT THE REFERENCE SIGNAL HAS BOTH A DESIRED RELATIONSHIP AND IS DEPENDENT UPON THE EXTERNAL VOLTAGE.

A. The Standard of Review.

As this Court succinctly stated in In re Bigio, 381 F.3d 1320, 1324 (Fed. Cir. 2004):

> Claim construction is a matter of law that this court reviews without deference. Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1454 (Fed. Cir. 1998) (en banc). During prosecution, however, the PTO gives claims their "broadest reasonable interpretation." In re Hyatt, 211 F.3d 1367, 1372 (Fed. Cir. 2000). Accordingly, this court reviews the "reasonableness" of the PTO's disputed claim term interpretations. In re Morris, 127 F.3d 1048, 1055 (Fed. Cir. 1997).

B. The Board's construction of two limitations of the claim to mean the same thing is unreasonable.

Claim 223 recites that the reference signal has "a desired relationship with the external signal" and that the reference signal "is dependent upon said external voltage [signal]." It is possible for the reference signal to have a desired relationship with the external signal, and not be dependent upon the external signal. It is also possible for the reference signal to be dependent upon the external signal, but not have a desired relationship with that signal. These two limitations do not mean the same thing.

An example of a graph showing the external voltage and the reference signed is found in FIG. 36B of the application as filed (JP00086) and is reproduced below.

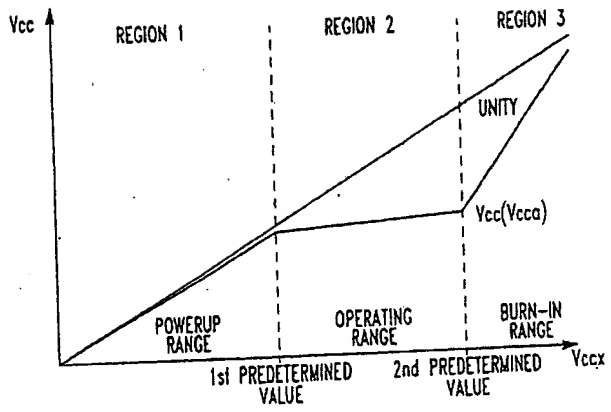


FIG. 36B

As seen from FIG. 36B, the reference signal may be said to be dependent upon the external voltage because the reference signal does not begin to be produced until the external voltage is applied. It can also be said that the reference signal has a desired relationship with the external voltage because, from a value of zero to a first predetermined value, the two signals have the same value. Between a first predetermined value and a second predetermined value, the reference signal is substantially flat even though the external voltage increases. After the second predetermined value, the reference signal continues to increase as the external voltage increases. Thus, FIG. 36B of the application as filed illustrates one example of how the reference signal may be dependent upon the external voltage and, additionally, have a desired relationship with the external voltage. Applicants' FIG. 36B should be contrasted with figure 5 of Morishita. (JP00228).

In Morishita, the circuit producing the reference signal does not become operative until the external signal reaches a predetermined value. After the predetermined value is reached, the circuit of Morishita becomes active to produce the reference signal, but there is no predetermined relationship between the two signals. That is clear from Morishita, column 2, lines 16-20, which recites:

> Reference voltage generating circuit VRG, of which internal structure will be described later in detail, generates the reference voltage Vref *independent of the external power supply voltage* EXVcc when the voltage EXVcc is at least at a prescribed voltage level. (emphasis added) JP00236.

Thus, Morishita clearly teaches that the circuit producing the reference signal is not operative until a predetermined value for the external voltage is reached, but thereafter, the circuit operates independently of the external signal.

While it may be said that Morishita discloses a dependence between the reference signal and the external signal, it is clear that there is no relationship between those two signals. In fact, Morishita explicitly teaches the opposite when it states that the reference voltage Vref is generated independently of the external power supply voltage. In view of those clear and express teachings in Morishita, the following conclusion of the Board cannot be supported.

> In other words, the fact alone that a reference voltage in Morishita may not be produced until an external voltage exceeds a prescribed level establishes, in our view, a desired relationship with such external voltage. Similarly, the reliance on the attaining a voltage level by the external

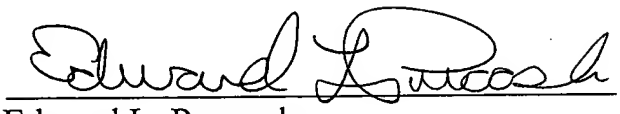
> voltage in Morishita before a reference voltage is produced makes Morishita's reference voltage dependent on the external voltage as claimed. JP00007 – JP00008

It is clear from the Board's reasoning that the Board construed "desired relationship" to mean the same thing as "dependent upon." It was legal error and unreasonable for the Board to construe two limitations of the claim to mean the same thing – every word adds meaning. Harris Corp. v. IXYS Corp., 114 F.3d 1149, 43 USPQ 2d 1018 (Fed. Cir. 1997) "that construction would contribute nothing but meaningless verbiage to the definition of the claimed invention"; Elekta Instruments S.A. v. O.U.R. Scientific Int'l, Inc., 214 F.3d 1302, 1307, 54 USPQ 2d 1910, 1913 (Fed. Cir. 2000) "any other conclusion renders the reference to 30 degrees superfluous."; Unique Concepts, Inc. v. Brown, 939 F.2d 1558, 19 USPQ 2d 1500 (Fed. Cir. 1991); General American Transportation Corp. v. Cryo-Trans, Inc., 93 F.3d 766, 39 USPQ 2d 1801 (Fed. Cir. 1996). The Board compounded that error by then concluding that both of those limitations were met by a single teaching in the prior art. It is respectfully submitted that this court should reverse the Board by holding that the phrases "desired relationship" and "dependent upon" do not mean the same thing, and therefore the teaching of Morishita fails to anticipate claim 223.

CONCLUSION

For the foregoing reasons, it is respectfully submitted that this Court reverse the decision of the Board.

Respectfully submitted,



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Dated: April 5, 2006

ADDENDUM

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte BRENT KEETH and LAYNE G. BUNKER

Appeal No. 2005-1576
Application No. 09/885,217

ON BRIEF

Before RUGGIERO, GROSS, and BARRY, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejecion of claims 223, 225, 228-237, 247-250, 496, and 499-515.

The claimed invention relates to a voltage reference circuit for supplying a reference voltage in which an active reference circuit receives an external voltage and produces a reference signal having a desired relationship with the external voltage. The active reference circuit includes a current source utilizing a current mirror to provide current to a diode stack having an adjustable impedance. Further included is a unity gain amplifier

acting in response to the reference signal, which is dependent on the external voltage, for producing the reference voltage.

Claim 223 is illustrative of the invention and reads as follows:

223. A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:
an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage, said active reference circuit comprising a current source utilizing a current mirror for providing current to a diode stack having an adjustable impedance, wherein said reference signal is dependent upon said external voltage; and
a unity gain amplifier responsive to said reference signal for producing the reference voltage.

The Examiner relies on the following prior art:

Hayakawa et al. (Hayakawa)	5,184,031	Feb. 02, 1993
Park	5,448,199	Sep. 05, 1995
Morishita et al. (Morishita)	5,757,175	May 26, 1998 (filed Jan. 13, 1997)
Zarrabian et al. (Zarrabian)	5,838,076	Nov. 17, 1998 (filed Nov. 21, 1996)
Tsay et al. (Tsay)	6,127,881	Oct. 03, 2000 (filed May 31, 1994)

Claims 223 and 511 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by Morishita. Claims 225, 496, 499, 500, and 514 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Morishita in view of Zarrabian.

Claims 228-230 and 501-503 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Morishita in view of Park. Claims 231, 504, 512, and 515 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsay in view of Morishita. Claims 232, 233, 505, and 506 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayakawa in view of Tsay and Morishita. Claims 234-237, 247-250, 507-510, and 513 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayakawa in view of Tsay, Morishita, and Park.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs[1] and Answer for their respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner, the arguments in support of the rejections, and the evidence of anticipation and obviousness relied upon by the Examiner as support for the

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[1] The Appeal Brief was filed March 18, 2004. In response to the Examiner's Answer mailed June 3, 2004, a Reply Brief was filed July 19, 2004, which was acknowledged and entered by the Examiner as indicated in the communication mailed November 5, 2004.

rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the disclosure of Morishita fully meets the invention as recited in claims 223 and 511. In addition, we are of the opinion that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 225 and 228-237, 247-250, 496, 499-510, and 512-515. Accordingly, we affirm.

At the outset, we note that Appellants indicate (Brief, page 3) that, for purposes of this appeal, all claims will stand or fall together. Consistent with this indication, Appellants' arguments in the Brief are directed solely to features which are set forth in independent claim 223. Accordingly, we will select independent claim 223 as the representative claim for all the claims on appeal, and claims 225, 228-237, 247-250, 496, and 499-515 will stand or fall with claim 223. Note In re King, 801 F.2d

1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

We note that anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

At pages 3, 4, 10, and 11 of the Answer, the Examiner indicates how the various limitations in representative claim 223 are read on the disclosure of Morishita. In particular, the Examiner directs attention to the illustrations in Figures 17-19 of Morishita along with the accompanying description beginning at column 1, line 66 of Morishita.

In our view, the Examiner's analysis is sufficiently reasonable that we find that the Examiner has as least satisfied the burden of presenting a prima facie case of anticipation. The burden is, therefore, upon Appellants to come forward with

evidence and/or arguments which persuasively rebut the Examiner's prima facie case. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived [see 37 CFR § 41.37(c)(1)(vii)].

Appellants' arguments in response assert that the Examiner has not shown how each of the claimed features are present in the disclosure of Morishita so as to establish a case of anticipation. In particular, Appellants contend that, in contrast to the claimed invention, "Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier for producing a reference voltage in response to a reference signal." (Brief, page 4).

After careful review of the Morishita reference in light of the arguments of record, however, we are in general agreement with the Examiner's position as stated in the Answer. We find no arguments from Appellants that convince us of any error in the Examiner's position which, considering the entire circuitry illustrated in Figure 17 of Morishita as a voltage reference circuit, asserts that the amplifier circuit comprising elements

CMP and DT in Morishita is a unity gain amplifier. We further agree with the Examiner that Morishita's unity gain amplifier produces a reference voltage as claimed since the reference voltage Vref is maintained at the internal power supply voltage INVcc level.

We further find to be unpersuasive Appellants' argument (Reply Brief, page 2) that, unlike the claimed invention, the reference signal in Morishita does not have a desired relationship with the external voltage. In support of this contention, Appellants rely on certain portions of Morishita which, in their view, suggest that no reference voltage is produced until the external voltage exceeds a predetermined voltage level.

It is our opinion, however, that even assuming, arguendo, that Appellants' characterization of the operation of the circuitry of Morishita is correct, such circuit operation in fact satisfies the language of claim 223. In other words, the fact alone that a reference voltage in Morishita may not be produced until an external voltage exceeds a prescribed level establishes, in our view, a desired relationship with such external voltage.

Similarly, the reliance on the attaining of a voltage level by the external voltage in Morishita before a reference voltage is produced makes Morishita's reference voltage dependent on the external voltage as claimed.

In view of the above discussion, since the Examiner's prima facie case of anticipation has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 102(e) rejection of representative claim 223, as well as claims 225, 228-237, 247-250, 496, and 499-515 which fall with claim 223, is sustained. Therefore, the decision of the Examiner rejecting claims 223, 225, 228-237, 247-250, 496, and 499-515 is affirmed.

No time period for taking any subsequent action in onnection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv)(effective September 13, 2004).

AFFIRMED

JOSEPH F. RUGGIERO)
Administrative Patent Judge)
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ANITA PELLMAN GROSS) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
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)
LANCE LEONARD BARRY)
Administrative Patent Judge)

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Appeal No. 2005-1576
Application No. 09/885,217

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CERTIFICATE OF FILING AND SERVICE

I hereby certify that on this 7th day of April, 2006, two bound copies of the foregoing Brief of Appellant were served via U.S. Mail, postage prepaid, to the following:

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I also certify that on this 7th day of April, 2006, the required number of copies of the foregoing Brief of Appellant were hand filed at the Office of the Clerk, United States Court of Appeals for the Federal Circuit.

Filing and service were performed under instruction of counsel.

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